WHAT IS CLAIMED IS:

1. A variable resistance device comprising:

a first variable resistance circuit including n resistors connected in series forming a first series-resistor circuit and analog switches connected between one terminal of the series-resistor circuit and respective nodes of the resistors of the series-resistor circuit, n being an integer of 2 or more, the analog switches being on/off controlled by an output signal of a counter to stepwise change a resistance value of the first variable resistance circuit;

a second variable resistance circuit one terminal of which is connected to the one terminal of the first series-resistor circuit of the first variable resistance circuit, the second variable resistance circuit including a second series-resistor circuit of a first resistor and a second resistor which have a predetermined resistance ratio therebetween, one terminal of the first resistor being connected to one terminal of the second resistor, the other terminal of the first resistor being connected to the one terminal of the series-resistor circuit of the first variable resistance circuit, a third series-resistor circuit of a plurality of resistors, one terminal of third series-resistor circuit being connected to the other terminal of the second resistor, a plurality of analog switches connected between the other terminal of the first

resistor and nodes of the respective resistors of the third series-resistor circuit, an analog switch connected between the other terminal of the third series-resistor circuit and a node of the first resistor and the second resistor and controlled by an output signal of a counter, an analog switch connected between a node of resistors of the third series-resistor circuit and the node of the first resistor and the second resistor and controlled by an output signal of a counter, and

a short-circuiting analog switch connected between the other terminal of series-resistor circuit of the first variable resistance circuit and the other terminal of the second resistor of the second variable resistance circuit and controlled by an output signal of a counter to make a short-circuit therebetween.

2. The variable resistance device according to claim 1 wherein the n resistors of the first series-resistor circuit of the first variable resistance circuit have a resistance r substantially equal to one another.

3. The variable resistance device according to claim 1, wherein each of the analog switches of the first variable resistance circuit and the second variable resistance circuit comprises an N channel MOS transistor alone or a P channel MOS transistor alone, and the short-circuiting analog switch for

short-circuiting the series-resistor circuit of the first variable resistance circuit and the second resistor of the second variable resistance circuit comprises a combination of an N channel MOS transistor and a P channel MOS transistor.

4. The variable resistor device according to claim 1, wherein a resistor is inserted in series between the one terminal of the first series-resistor circuit of the first variable resistance circuit and that resistor of the resistors of the first series-resistor circuit which is closest to the one terminal of the first series-resistor circuit, the inserted resistor having a resistance substantially equal to an on-resistance of each of the analog switches of the first variable resistance circuit.

5. A zero-data-detection mute circuit of an output section of a one-bit D/A converter in which a multibit digital signal is converted into a one-bit signal via a modulator, the one-bit signal is outputted in a form of analog signal via an inverting type amplifier of an analog low-pass filter, a counter is operated when detecting that the multibit digital signals are all zero for a predetermined time period to decrease stepwise a resistance of a feedback resistor circuit of the inverting type amplifier of the analog low-pass filter and finally make a short-circuit both terminals of the feedback resistor circuit according to

an output of the counter to fix an output of the inverting type amplifier to a reference potential, the feedback resistor circuit comprising:

a first variable resistance circuit including n resistors connected in series forming a first series-resistor circuit and analog switches connected between one terminal of the series-resistor circuit and respective nodes of the resistors of the series-resistor circuit, n being an integer of 2 or more, the analog switches being on/off controlled by an output signal of a counter to stepwise change a resistance value of the first variable resistance circuit;

a second variable resistance circuit one terminal of which is connected to the one terminal of the first series-resistor circuit of the first variable resistance circuit, the second variable resistance circuit including a second series-resistor circuit of a first resistor and a second resistor which have a predetermined resistance ratio therebetween, one terminal of the first resistor being connected to one terminal of the second resistor, the other terminal of the first resistor being connected to the one terminal of the series-resistor circuit of the first variable resistance circuit, a third series-resistor circuit of a plurality of resistors, one terminal of third series-resistor circuit being connected to the other terminal of the second resistor, a plurality of analog switches

connected between the other terminal of the first resistor and nodes of the respective resistors of the third series-resistor circuit, an analog switch connected between the other terminal of the third series-resistor circuit and a node of the first resistor and the second resistor and controlled by an output signal of a counter, an analog switch connected between a node of resistors of the third series-resistor circuit and the node of the first resistor and the second resistor and controlled by an output signal of a counter, and

a short-circuiting analog switch connected between the other terminal of series-resistor circuit of the first variable resistance circuit and the other terminal of the second resistor of the second variable resistance circuit and controlled by an output signal of a counter to make a short-circuit therebetween.

6. The zero-data-detection mute circuit according to claim 5, wherein the n resistors of the first series-resistor circuit of the first variable resistance circuit have a resistance r substantially equal to one another.

7. The zero-data-detection mute circuit according to claim 5, wherein each of the analog switches of the first variable resistance circuit and the second variable resistance circuit comprises an N channel MOS transistor alone or a P channel MOS transistor alone,

and the short-circuiting analog switch for short-circuiting the series-resistor circuit of the first variable resistance circuit and the second resistor of the second variable resistance circuit comprises a combination of an N channel MOS transistor and a P channel MOS transistor.

8. The zero-data-detection mute circuit according to claim 5, wherein a resistor is inserted in series between the one terminal of the first series-resistor circuit of the first variable resistance circuit and that resistor of the resistors of the first series-resistor circuit which is closest to the one terminal of the first series-resistor circuit, the inserted resistor having a resistance substantially equal to an on-resistance of each of the analog switches of the first variable resistance circuit.

9. A variable resistance device comprising:

a first variable resistance circuit including n resistors connected in series forming a series-resistor circuit and analog switches connected between one terminal of the series-resistor circuit and respective nodes of the resistors of the series-resistor circuit, n being an integer of 2 or more, the n resistors each having a resistance value of r, the analog switches being on/off controlled by an output signal of a counter to stepwise change a resistance value of the first variable resistance circuit from 0 to $n \cdot r$; and

a second variable resistance circuit, the second variable resistance circuit including:

a first resistor having a resistance value of 0.53r,

a second resistor having a resistance value of 0.47r one terminal of which is connected to one terminal of the first resistor and the other terminal of which is connected to one terminal of the series-resistor circuit of the first variable resistance circuit,

a third resistor having a resistance value of r/7 one terminal of which is connected to the other terminal of the first resistor,

a first analog switch one terminal of which is connected to the other terminal of the third resistor, and the other terminal of which is connected to the other terminal of the second resistor, a fourth resistor having a resistance value of 4r/21 one terminal of which is connected to the other terminal of the third resistor,

a second analog switch one terminal of which is connected to the other terminal of the fourth resistor, and the other terminal of which is connected to the other terminal of the second resistor,

a fifth resistor having a resistance value of 4r/15 one terminal of which is connected to the other terminal of the fourth resistor,

a third analog switch one terminal of which is connected to the other terminal of the fifth resistor, and the other terminal of which is connected to the other terminal of the second resistor,

a sixth resistor having a resistance value of 2r/5 one terminal of which is connected to the other terminal of the fifth resistor,

a fourth analog switch one terminal of which is connected to the other terminal of the sixth resistor, and the other terminal of which is connected to the other terminal of the second resistor,

a seventh resistor having a resistance value of 2r/3 one terminal of which is connected to the other terminal of the sixth resistor,

a fifth analog switch one terminal of which is connected to the other terminal of the seventh resistor, and the other terminal of which is connected to the other terminal of the second resistor,

a sixth analog switch one terminal of which is connected to the other terminal of the fifth resistor, and the other terminal of which is connected to the one terminal of the first resistor,

a seventh analog switch one terminal of which is connected to the other terminal of the seventh resistor, and the other terminal of which is connected to the one terminal of the first resistor, and

an eighth analog switch connected between the

other terminal of the series-resistor circuit of the first variable resistance circuit and the other terminal of the first resistor of the second variable resistance circuit to make a short-circuit therebetween.

10. The variable resistance device according to claim 9, wherein in the second variable resistance circuit,

an on-resistance of the first analog switch is set to R7,

an on-resistance of the second analog switch is set to R6,

an on-resistance of the third analog switch is set to R5,

an on-resistance of the fourth analog switch is set to R4,

an on-resistance of the fifth analog switch is set to R3,

an on-resistance of the sixth analog switch is set to R2, and

an on-resistance of the seventh analog switch is set to R1 in which R2 becomes equal to R5 and R1 becomes equal to R3, and

a resistance value of the third resistance is set to r/7-R7,

a resistance value of the fourth resistance is set to 4r/21+R7-R6,

a resistance value of the fifth resistance is set to 4r/15+R6-R5,

a resistance value of the sixth resistance is set to 2r/5+R5-R4, and

a resistance value of the seventh resistance is set to 2r/3+R4-R3.

11. The variable resistance device according to claim 10, wherein

on-resistances of all of the analog switches in the first variable resistance circuit are equal to one another,

a resistor is inserted in series between the one terminal of the series-resistor circuit of the first variable resistance circuit and the other terminal of the second resistor of the second variable resistance circuit, a resistance of the inserted resistor being equal to the on-resistance of each of the analog switches in the first variable resistor circuit, an on-resistance value of the eighth analog switch being equal to the on-resistance of each of the analog switches in the first variable resistor circuit, and

a ninth analog switch is provided in parallel with the eighth analog switch, the ninth analog switch is turned on one step after the eighth analog switch is turned on to turn to a mute-on and the eighth analog switch is turned off one step after the ninth analog switch is turned off to turn to a mute-off.

12. The variable resistance device according to claim 11, wherein

on-resistance of the eighth analog switch is equal to an on-resistance of each of the analog switches in the first variable resistance circuit,

a ninth analog switch and a tenth analog switch are provided in parallel with the eighth analog switch, the ninth analog switch is turned on one step after the eighth analog switch is turned on, and the tenth analog switch is turned on one step after the ninth analog switch is turned on when a mute is turned on,

the ninth analog switch is turned off one step after the tenth analog switch is turned off and the eighth analog switch is turned off one step after the ninth analog switch is turned off when a mute is turned off, and

the ninth analog switch and the tenth analog switch are turned on when the mute is turned on.

13. The variable resistance device according to claim 9, wherein each of the analog switches of the first variable resistance circuit and the second variable resistance circuit comprises an N channel MOS transistor alone or a P channel MOS transistor alone, and the eighth analog switch comprises a combination of an N channel MOS transistor and a P channel MOS transistor.

14. A zero-data-detection mute circuit of an

output section of a one-bit D/A converter in which a multibit digital signal is converted into a one-bit signal via a modulator, the one-bit signal is outputted in a form of analog signal via an inverting type amplifier of an analog low-pass filter, a counter is operated when detecting that the multibit digital signals are all zero for a predetermined time period to decrease stepwise a resistance of a feedback resistor circuit of the inverting type amplifier of the analog low-pass filter and finally make a short-circuit both terminals of the feedback resistor circuit according to an output of the counter to fix an output of the inverting type amplifier to a reference potential, the feedback resistor circuit comprising:

a first variable resistance circuit including n resistors connected in series forming a series-resistor circuit and analog switches connected between one terminal of the series-resistor circuit and respective nodes of the resistors of the series-resistor circuit, n being an integer of 2 or more, the n resistors each having a resistance value of r, the analog switches being on/off controlled by an output signal of a counter to stepwise change a resistance value of the first variable resistance circuit from 0 to $n \cdot r$; and

a second variable resistance circuit, the second variable resistance circuit including:

a first resistor having a resistance value of

0.53r,

a second resistor having a resistance value of 0.47r one terminal of which is connected to one terminal of the first resistor and the other terminal of which is connected to one terminal of the series-resistor circuit of the first variable resistance circuit,

a third resistor having a resistance value of r/7 one terminal of which is connected to the other terminal of the first resistor,

a first analog switch one terminal of which is connected to the other terminal of the third resistor, and the other terminal of which is connected to the other terminal of the second resistor, a fourth resistor having a resistance value of 4r/21 one terminal of which is connected to the other terminal of the third resistor,

a second analog switch one terminal of which is connected to the other terminal of the fourth resistor, and the other terminal of which is connected to the other terminal of the second resistor,

a fifth resistor having a resistance value of 4r/15 one terminal of which is connected to the other terminal of the fourth resistor,

a third analog switch one terminal of which is connected to the other terminal of the fifth resistor, and the other terminal of which is connected to the

other terminal of the second resistor,

a sixth resistor having a resistance value of 2r/5 one terminal of which is connected to the other terminal of the fifth resistor,

a fourth analog switch one terminal of which is connected to the other terminal of the sixth resistor, and the other terminal of which is connected to the other terminal of the second resistor,

a seventh resistor having a resistance value of 2r/3 one terminal of which is connected to the other terminal of the sixth resistor,

a fifth analog switch one terminal of which is connected to the other terminal of the seventh resistor, and the other terminal of which is connected to the other terminal of the second resistor,

a sixth analog switch one terminal of which is connected to the other terminal of the fifth resistor, and the other terminal of which is connected to the one terminal of the first resistor,

a seventh analog switch one terminal of which is connected to the other terminal of the seventh resistor, and the other terminal of which is connected to the one terminal of the first resistor, and

an eighth analog switch connected between the other terminal of the series-resistor circuit of the first variable resistance circuit and the other terminal of the first resistor of the second variable

resistance circuit to make a short-circuit therebetween.

15. The zero-data-detection mute circuit according to claim 14, wherein in the second variable resistance circuit,

an on-resistance of the first analog switch is set to R7,

an on-resistance of the second analog switch is set to R6,

an on-resistance of the third analog switch is set to R5,

an on-resistance of the fourth analog switch is set to R4,

an on-resistance of the fifth analog switch is set to R3,

an on-resistance of the sixth analog switch is set to R2, and

an on-resistance of the seventh analog switch is set to R1 in which R2 becomes equal to R5 and R1 becomes equal to R3, and

a resistance value of the third resistance is set to r/7-R7,

a resistance value of the fourth resistance is set to 4r/21+R7-R6,

a resistance value of the fifth resistance is set to 4r/15+R6-R5,

a resistance value of the sixth resistance is set

to 2r/5+R5-R4, and

a resistance value of the seventh resistance is set to 2r/3+R4-R3.

16. The zero-data-detection mute circuit according to claim 15, wherein

on-resistances of all of the analog switches in the first variable resistance circuit are equal to one another,

a resistor is inserted in series between the one terminal of the series-resistor circuit of the first variable resistance circuit and the other terminal of the second resistor of the second variable resistance circuit, a resistance of the inserted resistor being equal to the on-resistance of each of the analog switches in the first variable resistor circuit, an on-resistance value of the eighth analog switch being equal to the on-resistance of each of the analog switches in the first variable resistor circuit, and

a ninth analog switch is provided in parallel with the eighth analog switch, the ninth analog switch is turned on one step after the eighth analog switch is turned on to turn to a mute-on and the eighth analog switch is turned off one step after the ninth analog switch is turned off to turn to a mute-off.

17. The zero-data-detection mute circuit according to claim 16, wherein

on-resistance of the eighth analog switch is equal

to an on-resistance of each of the analog switches in the first variable resistance circuit,

a ninth analog switch and a tenth analog switch are provided in parallel with the eighth analog switch, the ninth analog switch is turned on one step after the eighth analog switch is turned on, and the tenth analog switch is turned on one step after the ninth analog switch is turned on when a mute is turned on,

the ninth analog switch is turned off one step after the tenth analog switch is turned off and the eighth analog switch is turned off one step after the ninth analog switch is turned off when a mute is turned off, and

the ninth analog switch and the tenth analog switch are turned on when the mute is turned on.

18. The zero-data-detection mute circuit according to claim 14, wherein each of the analog switches of the first variable resistance circuit and the second variable resistance circuit comprises an N channel MOS transistor alone or a P channel MOS transistor alone, and the eighth analog switch comprises a combination of an N channel MOS transistor and a P channel MOS transistor.

19. A zero-data-detection mute circuit of an output section of a one-bit D/A converter, comprising:

an analog low-pass filter including an inverting type amplifier, configured to pass an analog-converted

output of a one-bit D/A converter;

zero-data-detecting circuit configured to detect that an input digital signal inputted to the D/A converter is 0-level data;

a counter configured to receive an output signal of the zero-data-detecting circuit and generate an output signal when detecting that the digital signals inputted to the D/A converter are all zero for a predetermined time period; and

a decoder configured to decode the output signal of the counter and decrease stepwise a resistance of a feedback resistor circuit of the inverting type amplifier of the analog low-pass filter and finally make a short-circuit both terminals of the feedback resistor circuit to fix an output of the analog low-pass filter to a reference potential, the feedback resistor circuit including a first variable resistance circuit and a second variable resistance circuit, wherein

the first variable resistance circuit includes n resistors connected in series forming a series-resistor circuit and analog switches connected between one terminal of the series-resistor circuit and respective nodes of the resistors of the series-resistor circuit, n being an integer of 2 or more, the n resistors each having a resistance value of r, the analog switches being on/off controlled by an output signal of a

counter to stepwise change a resistance value of the first variable resistance circuit from 0 to $n \cdot r$; and

the second variable resistance circuit includes:

a first resistor having a resistance value of 0.53r,

a second resistor having a resistance value of 0.47r one terminal of which is connected to one terminal of the first resistor and the other terminal of which is connected to one terminal of the series-resistor circuit of the first variable resistance circuit,

a third resistor having a resistance value of r/7 one terminal of which is connected to the other terminal of the first resistor,

a first analog switch one terminal of which is connected to the other terminal of the third resistor, and the other terminal of which is connected to the other terminal of the second resistor,

a fourth resistor having a resistance value of 4r/21 one terminal of which is connected to the other terminal of the third resistor,

a second analog switch one terminal of which is connected to the other terminal of the fourth resistor, and the other terminal of which is connected to the other terminal of the second resistor,

a fifth resistor having a resistance value of 4r/15 one terminal of which is connected to the other

terminal of the fourth resistor,

a third analog switch one terminal of which is connected to the other terminal of the fifth resistor, and the other terminal of which is connected to the other terminal of the second resistor,

a sixth resistor having a resistance value of 2r/5 one terminal of which is connected to the other terminal of the fifth resistor,

a fourth analog switch one terminal of which is connected to the other terminal of the sixth resistor, and the other terminal of which is connected to the other terminal of the second resistor,

a seventh resistor having a resistance value of 2r/3 one terminal of which is connected to the other terminal of the sixth resistor,

a fifth analog switch one terminal of which is connected to the other terminal of the seventh resistor, and the other terminal of which is connected to the other terminal of the second resistor,

a sixth analog switch one terminal of which is connected to the other terminal of the fifth resistor, and the other terminal of which is connected to the one terminal of the first resistor,

a seventh analog switch one terminal of which is connected to the other terminal of the seventh resistor, and the other terminal of which is connected to the one terminal of the first resistor, and

an eighth analog switch connected between the other terminal of the series-resistor circuit of the first variable resistance circuit and the other terminal of the first resistor of the second variable resistance circuit to make a short-circuit therebetween.

20. A zero-data-detection mute circuit of an output section of a one-bit D/A converter, comprising:

an analog low-pass filter including an inverting type amplifier, configured to pass an analog-converted output of a one-bit D/A converter;

zero-data-detecting circuit configured to detect that an input digital signal inputted to the D/A converter is 0-level data;

a counter configured to receive an output signal of the zero-data-detecting circuit and generate an output signal when detecting that the digital signals inputted to the D/A converter are all zero for a predetermined time period; and

a decoder configured to decode the output signal of the counter and decrease stepwise a resistance of a feedback resistor circuit of the inverting type amplifier of the analog low-pass filter and finally make a short-circuit both terminals of the feedback resistor circuit to fix an output of the analog low-pass filter to a reference potential, wherein the feedback resistor circuit includes:

a first variable resistance circuit including n resistors connected in series forming a first series-resistor circuit and analog switches connected between one terminal of the series-resistor circuit and respective nodes of the resistors of the series-resistor circuit, n being an integer of 2 or more, the analog switches being on/off controlled by an output signal of a counter to stepwise change a resistance value of the first variable resistance circuit;

a second variable resistance circuit one terminal of which is connected to the one terminal of the first series-resistor circuit of the first variable resistance circuit, the second variable resistance circuit including a second series-resistor circuit of a first resistor and a second resistor which have a predetermined resistance ratio therebetween, one terminal of the first resistor being connected to one terminal of the second resistor, the other terminal of the first resistor being connected to the one terminal of the series-resistor circuit of the first variable resistance circuit, a third series-resistor circuit of a plurality of resistors, one terminal of third series-resistor circuit being connected to the other terminal of the second resistor, a plurality of analog switches connected between the other terminal of the first resistor and nodes of the respective resistors of the third series-resistor circuit, an analog switch

connected between the other terminal of the third series-resistor circuit and a node of the first resistor and the second resistor and controlled by an output signal of a counter, an analog switch connected between a node of resistors of the third series-resistor circuit and the node of the first resistor and the second resistor and controlled by an output signal of a counter, and

a short-circuiting analog switch connected between the other terminal of series-resistor circuit of the first variable resistance circuit and the other terminal of the second resistor of the second variable resistance circuit and controlled by an output signal of a counter to make a short-circuit therebetween.

21. The variable resistance device according to claim 2, wherein the analog switches being on/off controlled to stepwise change the resistance value of the first variable resistance circuit from 0 to nr in units of r.

22. The zero-data-detection mute circuit according to claim 6, wherein the analog switches being on/off controlled to stepwise change the resistance value of the first variable resistance circuit from 0 to nr in units of r.

23. The variable resistance device according to claim 9, wherein a resistance value between the other terminal of the first resistor having the resistance

value of 0.53r and the other end of the second resistor having the resistance value of 0.47r is changed from r/8 to r in units of r/8.

24. The zero-data-detection mute circuit according to claim 14, wherein a resistance value between the other terminal of the first resistor having the resistance value of 0.53r and the other end of the second resistor having the resistance value of 0.47r is changed from r/8 to r in units of r/8.

25. The zero-data-detection mute circuit according to claim 19, wherein a resistance value between the other terminal of the first resistor having the resistance value of 0.53r and the other end of the second resistor having the resistance value of 0.47r is changed from r/8 to r in units of r/8.

26. The zero-data-detection mute circuit according to claim 25, wherein a resistance value between the other terminal of the first resistor having the resistance value of 0.53r and the other end of the second resistor having the resistance value of 0.47r is changed from r/8 to r in units of r/8.

output signal of a counter to make a short-circuit therebetween.

27. The zero-data-detection mute circuit according to claim 5, wherein the modulator comprises a ΣΔ modulator.

28. The zero-data-detection mute circuit according

to claim 14, wherein the modulator comprises a $\Sigma\Delta$ modulator.